


PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) I-2-0459.1US	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____ Signature _____ Typed or printed name _____		Application Number 10/799,951	Filed March 12, 2004
First Named Inventor Haim et al.		Examiner Aristocratis Fotakis	
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.		<div style="text-align: center;">  Signature Robert I. Solomon Typed or printed name </div> <div style="text-align: center;"> 215-568-6400 Telephone number </div> <div style="text-align: center;"> September 1, 2009 Date </div>	
I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/98) <input checked="" type="checkbox"/> attorney or agent of record. Registration number 61,761		<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.			
<input type="checkbox"/> *Total of _____ forms are submitted.			

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the **PATENT APPLICATION** of:

Haim et al.

Application No.: 10/799,951

Confirmation No.: 8032

Filed: March 12, 2004

For: ENHANCED AUTOMATIC GAIN
CONTROL MECHANISM FOR
TIME-SLOTTED DATA
TRANSMISSIONS

Group: 2611

Examiner: Aristocratis Fotakis

Our File: I-2-0459.1US

Date: September 1, 2009

**ARGUMENTS ACCOMPANYING PRE-APPEAL BRIEF
REQUEST FOR REVIEW**

Mail Stop AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Pre-Appeal Brief Review is hereby requested in this patent application.

The pending claims specify methods and apparatus for using a gain control loop to also erase received data so that further processing of that data is not required.

Two independent claims are pending. Independent apparatus claim 12 is representative and specifies:

12. A receiver comprising:
 - a gain control loop configured to process samples of a data signal received with respect to a selected timeslot of a time frame including;
 - a gain control for applying a gain factor to samples of the data signal;

a saturation detection circuit configured to process samples from the gain control in selected groups to determine a number of samples within a group which exceed a saturation criteria;

a gain control adjustment circuit operatively associated with said gain control and said saturation detection circuit to adjust the gain factor applied by the gain control based in part on group saturation numbers determined by the saturation detection circuit while processing the data signal received with respect to the selected timeslot of time frame...; and

an erase circuit to compare the number of samples within a group of samples which exceed the saturation criteria to a threshold number and erase the group of samples if the number of samples within the group which exceed the saturation criteria is greater than the threshold number.

Independent method claim 3 and apparatus claim 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application Publication No. 2006/0014507 to Giancola et al. (hereinafter "Giancola") in view of U.S. Patent No. 6,721,547 to Husted et al. (hereinafter "Husted").

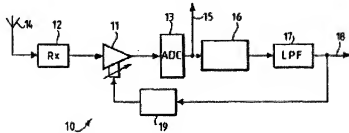
Both Giancola and Husted disclose gain control loop circuits, but neither disclose or suggest incorporating the claimed erase circuit therein. The final Action acknowledges that Giancola does not disclose the use of an erase circuit (Office Action (OA) page 4, paragraph 1) and that Husted does not specifically teach of erasing groups of samples (OA, page 4, paragraph 2).

The rejection states that Husted discloses an A/D maximum threshold which is the maximum saturation that a receiver can handle (OA, page 4, paragraph 2), then concludes:

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have compared the number with a threshold (A/D maximum threshold or A/D minimum threshold) so as to decide whether the data segment can be recovered (below A/D maximum threshold) or erased due to severe saturation (above A/D maximum threshold) being impossible to process.

However, there is no teaching or suggestion in the cited art for providing the claimed erase circuit that serves to compact the digital stream that is output for communication information retrieval processing.

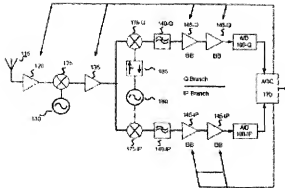
Figure 1 of Giancola, reproduced below is instructive:



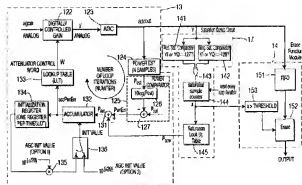
Element 15 indicates the output of the received signal from the gain control loop circuit after the ADC conversion by element 13 for processing to retrieve communication information from the digital stream output from the A/D converter. There is no teaching of erasing anything from that stream, but the processing circuitry (not shown) processes the entire digital stream. Information may not be successfully obtained from some portions of that digital stream, but the entire stream is output for processing.

The operation of the prior art gain control circuits merely operate to adjust the gain of the communication signal, for example, at amplifier 11 in the Figure above. The prior art gain control circuits do not attempt to modify/compact the digital stream output from the A/D converter.

Unlike the prior art, the digital stream output from the gain control loop circuit is modified by the erase circuit to provide a more compacted digital stream for processing as can be seen from application Figure 2 reproduced below:



Husted Figure 2



Application Figure 2


Husted's use of the ADC outputs is similar to the Applicants' use of the ADC 123 output for input to the POWER EST component 125 and Saturation Detection Circuit 17.

Husted does not, however, show outputs from the A/D converters 190 for the respective I and Q streams that are directed to the signal processing circuitry, since Husted is focused on teaching how the AGC circuit operates and such outputs (such as output 15 in Figure 1 of Giancola) are apparently assumed. This silence in Husted teaches away from any modification/compaction of the digital streams output from the A/D converters 190 that are directed to signal processing circuitry. This silence does not teach or suggest the erase circuit of independent claim 12.

For the above reasons, withdrawal of the rejection of claims based Giancola and Husted is respectfully requested.

Respectfully submitted,

Haim et al.

By 
Robert I. Solomon
Registration No. 61,761

Volpe and Koenig, P.C.
United Plaza
30 South 17th Street
Philadelphia, PA 19103-4009
Telephone: (215) 568-6400
Facsimile: (215) 568-6499
RIS/CFK/dml